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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/815,248	03/31/2004	William Hugh Cochran	ROC920030326US1	8154

7590 04/11/2006

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EXAMINER	
KERVEROS, JAMES C	

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 04/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/815,248	COCHRAN ET AL.	
	Examiner	Art Unit	
	JAMES C. KERVEROS	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/31/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a Non-Final Action in response to the instant U.S. Application filed 3/31/2004. Claims 1-20 are pending and presently under examination.

Specification

The abstract of the disclosure is objected, because of minor informalities. The Examiner is suggesting the following new abstract:

"A method and apparatus for detecting degradation, such as, array degradation and logic degradation, in integrated circuits (ICs) including application specific integrated circuits (ASICs). A monitor built-in self-test (MBIST) engine is coupled to at least one monitor element and is defined by predefined circuit elements in the integrated circuit. The MBIST engine is used for controlling operation of at least one monitor element for communicating with monitor bits to identify degradation of signal, timing and voltage margins". Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Pochmuller (US 6,295,237) issued: September 25, 2001.

Regarding independent Claims 1, 17, Pochmuller discloses a method and apparatus for a semiconductor memory configuration, such as a DRAM, in which redundant memory cells, bit lines and word lines are determined for failed memory cells, failed word lines and failed bit lines by a built-in-self-test (BIST) computing unit (see, Abstract), the method and apparatus comprising:

A semiconductor chip, word lines (WL), bit lines (BL) and a memory cell array disposed on the semiconductor chip and addressed via the word lines and the bit lines, the memory cell array having a multiplicity of memory cells (MC) Figure 1;

Redundant memory cells disposed on the semiconductor chip and addressed by the word lines and the bit lines, the redundant memory cells in an event of failed memory cells of the memory cell array replace the failed memory cells as spare memory cells, (See Summary of the Invention); and

A built-in-self-test (BIST) computing unit disposed on the semiconductor chip and connected to the memory cell array and the redundant memory cells, the BIST computing unit assigning the spare memory cells to the failed memory cells, the BIST computing unit having a register for storing addresses of the word lines and the bit lines of the failed memory cells, the BIST computing unit having a counter and, for each of the addresses, the counter increments a number relating to the failed memory cells as a hit value up to an upper limit, a corresponding one of the word lines or the bit

lines being replaced in an event of the upper limit being exceeded (See Figure 6 and Summary of the Invention).

Regarding Claims 2-5, 18-20, Pochmuller discloses in a test, the individual memory cell arrays are checked by driving their word lines and bit lines in order to determine defective memory cells, word lines and bit lines, where the results of the test are stored in a register 12. A built-in-self-test (BIST) computing unit 14 with a counter unit 15 for counting the hit values up to an upper limit then evaluates the results of the tests. The results finally being stored in the registers 12, after the conclusion of the tests and determines those redundant memory cells, bit lines and word lines which, as the spare memory cells, spare bit lines and spare word lines from the memory cell array 10, are intended to replace the defective memory cells, bit lines and word lines in the memory cell arrays (1, 2, . . , n). The replacement of the memory cells, the bit lines and the word lines is effected, for example, via corresponding bus lines 11, which connect the individual memory cell arrays to one another.

Regarding Claims 6-16, Pochmuller discloses semiconductor memory configuration, Figure 6, containing memory cell arrays (1, 2, . , n), constructed as shown in Figure 1. In this case, it is possible to provide the redundant bit lines and the word lines with the corresponding memory cells in each of the memory cell arrays (1, 2, . , n). Likewise, however, it is also possible to accommodate the redundant bit lines and the word lines with the corresponding memory cells in a separate memory cell array 10, which is placed proximate to the BIST computing unit 14.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

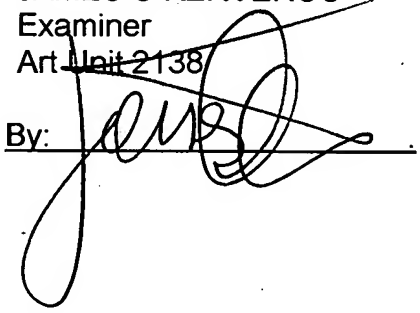
Huang et al. (US 6,640,321), discloses a method and apparatus using a BIST/BISR system for detecting degradation in a semiconductor memory device 20, including a memory array, which comprises regular memory rows 26 and redundant memory rows 28, Figure 6, including an execution unit (40), which implements the BIST/BISR routine of Figure 5 and controls test circuitry 36 over bi-directional bus 42, Figure 6; a (redundant memory rows 28) coupled to the (execution unit, 40) through test circuitry 36; the redundant memory rows 28 including a (redundant memory row, RRow 0-RRow p-1), Figures 2, 6. The BIST/BISR (40) tests the entire redundant memory (28) before implementing self-repair, as shown in the flowchart in Figure 5. The redundant memory is tested in the first BIST run 14, before testing the regular memory. A checkerboard test pattern is applied to the entire redundant memory, along with the contiguous row of regular memory. Identifying degradation of signal, timing and voltage margins, by recording redundant rows that fail during the BIST run 14, Figure 5.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C. KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JAMES C KERVEROS
Examiner
Art Unit 2138

By: 

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Date: 6 April 2006
Office Action: Non-Final Rejection